MINOS MINDER Module

Memory Map

MINOS MINDER Card VME Function Addresses 1/20/03

The MINOS MINDER Card is written to or read from through a MINOS TRIGGER-KEEPER Card that resides in the MINDER Crate.
The MINOS TRIGGER-KEEPER Card is accessed through a MINOS MASTER Card that resides in a MASTER Crate.
The MINOS MINDER's Card Address ID (switch SW1) **must not** be set to 31. This is reserved for the MINOS TRIGGER-KEEPER Card.
The MASTER Card must be in VME Mode.
The Address Modifier for interactions with the MINDER Crate is 09.
The VME Address that is received by the MASTER Card to interact with the MINDER Card is:

A31 A0
GGGG G000 0000 0001 01NN NNNT TTTT TT00

G = MASTER Card Geographical Address bits
N = MINDER Card Address ID bits (Set by switch SW1)
T = MINDER Card Function Address bits

MINDER Card Hex Address (h) Offset (A8-A2)	Function
h000	WRITE/READ – Card Disable Register (Disable = 1) D0 = Card Disable bit D15-D1 = 0 D31-D16 = Undefined
h004	WRITE/READ – External Source Flasher Trigger Window Delay and Width Register D7-D0 = Window Width (1-255 steps, 19ns/step) D15-D8 = Window Delay (0-255 steps, 19ns/step) D31-D16 = Undefined
h008	WRITE/READ – TCAL Flasher Trigger Window Delay and Width Register D7-D0 = Window Width (1-255 steps, 19ns/step) D15-D8 = Window Delay (0-255 steps, 19ns/step) D31-D16 = Undefined
h00C	READ only – Card ID D10-D0 = Card Serial Number (Hard-wired on the card) D15-D11 = Card Address ID (Set by switch SW1) D31-D16 = Undefined
h01C	WRITE only – Card Clear D31-D0 = No data needed

MINOS Near Detector
Front End Electronics

MINDER Module Functionality

Gary Drake
Argonne National Laboratory

Aug. 22, 2001

Revised Aug. 23, 2001

I. Trigger Sources

- Spill Gate Trigger
  - **SGATE** Comes from Clock System via MTM
  - Every MINDER has a Point-to-Point Connection with MTM

- Dynode Trigger
  - Comes from ASDLite Discriminators on KEEPER
  - Discriminated Signal from All PMTs Sent Onto Backplane as **nDTRIG[3:0]**
  - MINDERS Receive All 4 Signals
  - Slot Switch Settings on MINDER Tell It Which **nDTRIG** Signal to Respond To

- VME Trigger
  - Generated by Writing to a Register on the KEEPER (Which is a Location in Address Space on the MASTER)
  - KEEPER Generates **nDTRIG6**, Which is Sent onto MINDER Backplane
  - Use For:
    - Pedestals
    - DC Current Injection
    - Generating a Diagnostic Event

I. Trigger Sources (Cont.)

- **TCAL** Trigger
  - **TCAL** Comes from Clock System via MTM
  - Enables on MINDER Allow it to Respond to **TCAL** and Generate an Event

- **TCAL** Flasher Trigger
  - **TCAL** Comes from Clock System via MTM
  - Enables on MINDER Allow it to Form a Gate From **TCAL**
  - If Dynode Trigger Received Inside Gate, Event is Marked as a Flasher Event

- External Flasher Trigger
  - External Input on Keeper Can receive Trigger Signal from Flasher System
  - KEEPER Buffers and Sends onto MINDER Backplane as **nDTRIG4**
  - Received by All MINDERs on the Crate
  - Enables on MINDER Allow it to Form a Gate From **nDTRIG4**
  - If Dynode Trigger Received Inside Gate, Event is Marked as a Flasher Event

I. Trigger Sources (Cont.)

- External Process Trigger
  - External Input on Keeper Can receive Trigger Signal from an External Process
  - KEEPER Buffers and Sends onto MINDER Backplane as **nDTRIG5**
  - Received by All MINDERs on the Crate
  - Enables on MINDER Allow it to Respond

II. Summary of Trigger Signals

Trigger	Meaning	Used For
SGATE	Spill Gate	Trigger on Spill
nDTRIG0	Dynode Trigger PMT0	Cosmics, Flasher, PMT Noise
nDTRIG1	Dynode Trigger PMT1	Cosmics, Flasher, PMT Noise
nDTRIG2	Dynode Trigger PMT2	Cosmics, Flasher, PMT Noise
nDTRIG3	Dynode Trigger PMT3	Cosmics, Flasher, PMT Noise
nDTRIG4	Flasher Trigger Ext. Source	Forms Gate for Dynode Trigger
nDTRIG5	Ext. Process Trigger	Triggering from Ext. Process
nDTRIG6	VME Trigger	Pedestals, DC I Inj, Diagnostic Data
TCAL	Periodic Timing Signal	Diagnostics, Test Stands, Flasher

III. Mapping PMTs to Slots

- Address Switched on MINDER Correspond to Slot
- Switches Control Which of Dynode Signals (nDTRIG0 - nDTRIG3) to Respond To

Slot	nDTRIG
0- 2	None
3- 6	nDTRIG0
7-10	nDTRIG1
11-14	nDTRIG2
15-18	nDTRIG3
19-21	None

IV. Global Control Lines

- Set By Writing from MASTER to KEEPER
- Sourced By KEEPER Onto Backplane
- Received by All MINDERs

nCTRL	Meaning	Used For
nCTRL0	Mode Bit 0	Setting Mode
nCTRL1	Mode Bit 1	Setting Mode
nCTRL2	Mode Bit 2	Setting Mode
nCTRL3	SGATE Enable	Allow Response to SGATE - Norm Mode
nCTRL4	Dynode Trigger Enable	Allow Response to Dynode - Norm Mode
nCTRL5	Ext. Flash Trigger Enable	Allow Response to Ext Flash - Norm Mode
NCTRL6	TCAL Flash Enable	Allow Response to TCAL Flash Trig - Norm Mode
nCTRL7	Ext. Process Enable	Allow Response to Ext. Process Trig - Norm Mode

IV. Global Control Lines (Cont.)

- 3 Mode Bits → 8 States
- Only 1 State May Be Active at a Given Time

Mode		Meaning	Used For
000	0	OFF	Board Will Not Respond toTriggers
001	1	NORM Mode	Physics Uses nCTRL3-nCTRL7
010	2	PED Mode	Acquire Pedestals Uses VME Trigger
011	3	ICAL Mode	DC I Inj. Cal Uses VME Trigger
100	4	DIAG Mode	Diagnostic Event Uses VME Trigger
101	5	TCAL Trig 1	Trigger on TCAL DTRIG Sequence
110	6	TCAL Trig 2	Trigger on TCAL SGATE Sequence
111	7	QIE Reset	Generate QIE Reset Using TCAL

V. Data Types Defied

- 3 Data Type Bits → 8 Kinds
- Sent Along with Data

Data Type	Meaning	Set By
0	Pedestal	MODE[2:0] = 2 and nDTRIG6
1	ICAL	MODE [2:0] = 3 and nDTRIG6
2	Diagnostic	MODE [2:0] = 4 and nDTRIG6
3	TCAL (Not Flasher)	MODE [2:0] = 5 and nDTRIG6
4	Spill	MODE [2:0] = 1 and SGATE
5	Dynode	MODE [2:0] = 1 and nDTRIG*i*
6	Flasher	MODE [2:0] = 1 and nDTRIG*i*
7	Ext. Process	MODE [2:0] = 1 and nDTRIG5

VI. DAQ Priority Defined

- Problem:
  - Data Transmission from DTRIG Takes ~4.8 uSec = 256 RF Clock
  - Spill or Flash Can Come At Any Time
  - Need Method to Interrupt Lesser Important Processes

- 3 Levels of Priority, Used in NORM Mode Only

- Higher Priority Process Can Interrupt Lesser One

Priority	Meaning	Can Interrupt:
3	- Lowest Priority - Used for Dynode	- None - Ignored if Another Priority 1 in Progress
2	- 2nd Priority - Used Flasher & Ext. Proc.	- Priority 3 - Ignored if Another Priority 2 in Progress
1	- Highest Priority - Used for Spill	- Priority 2 & Priority 3 - Ignored if Another Priority 1 in Progress
N/A	- Pedestals, ICAL Diagnostic Mode, TCAL-Generated Event	- Does Not Interrupt - Cannot Be Interrupted - Ignores Triggers if in Progress

VII. DAQ Sequences

- 2 Kinds: DTRIG and SGATE
- Sequence Determined by Data Type

Sequence	Used For	# Time Slices
DTRIG	Cosimcs, Flasher, PMT Noise, Ext. Process, TCAL Trig 1	8
SGATE	Spill, Pedestals, ICAL, Diagnostic, TCAL Trig 2	~526 (?) (10 uSec)

VIII. Summary of Trigger Signal Processing

Trigger	Signal	nCTRL Value	Execution Delay	DAQ Sequence	Data Type	Priority
Spill	SGATE	1 (NORM) + 8 (SGATE) + (Other NORM)	No	SGATE	4	1
Dynode PMT0 (Cosmics, PMT Noise)	nDTRIG0	1 (NORM) + 16 (DYN En) + (Other NORM)	0-7 Clks DTRIG_DLY	DTRIG	5	3
Dynode PMT1 (Cosmics, PMT Noise)	nDTRIG1	1 (NORM) + 16 (DYN En) + (Other NORM)	0-7 Clks DTRIG_DLY	DTRIG	5	3

VIII. Summary of Trigger Signals (Cont.)

Trigger	Signal	nCTRL Value	Execution Delay	DAQ Sequence	Data Type	Priority
Flash Event From TCAL (Gate DYN Trig)	TCAL	1 (NORM) + 16 (DYN En) + 64 (TCAL) + (Other NORM)	0-255 TFLSH_DLY 0-255 TFLSH_GATE	DTRIG	6	2
Flash Event From Flash Sys (Gate DYN Trig)	nDTRIG4	1 (NORM) + 16 (DYN En) + 32 (Ext Flash) + (Other NORM)	0-255 EFLSH_DLY 0-255 EFLSH_GATE	DTRIG	6	2
Ext. Process Event	nDTRIG5	1 (NORM) + 128 (PROCEN) + (Other NORM)	0-255 PROC_DLY	DTRIG	7	2
QIE Reset From TCAL	TCAL	7	No	N/A	N/A	N/A